CLAIMS:

1. A receiver comprising:

an input configured to receive serial data;

an oscillator configured to generate phases of a clock; and

a retiming mechanism configured to receive said serial data and said phases of said clock, wherein said retiming mechanism includes circuitry for reducing timing uncertainties in said serial data by selecting a particular phase of said clock to be asserted to sample said serial data during a period of said serial data.

2. The receiver as recited in claim 1, wherein each particular phase of said clock to be asserted to sample said serial data during a particular period of said serial data corresponds to a particular retiming state.

3. The receiver as recited in claim 2, wherein each particular retiming state is paired with a particular synchronization state, wherein said particular synchronization state indicates which particular phase of said clock to assert at a given transition of said serial data signal.

4. The receiver as recited in claim 3, wherein said retiming mechanism comprises a first unit, wherein said first unit includes circuitry for generating logical values of each particular synchronization state / retiming state pair.

5. The receiver as recited in claim 4, wherein said first unit receives said phases of said clock and said serial data.

6. The receiver as recited in claim 5, wherein said first unit comprises a sample clock mechanism configured to sample values of said phases of said clock.

7. The receiver as recited in claim 6, wherein said first unit comprises a plurality of second units, wherein said sampled phase values are inputted to said plurality of second units, wherein said plurality of second units includes circuitry for generating said logical values of each particular synchronization state / retiming state pair.

8. The receiver as recited in claim 7, wherein said plurality of second units output said logical values of each particular synchronization state / retiming state pair to a completion detector, wherein said completion detector includes circuitry for generating a signal indicating a time to sample inputs of said completion detector.

9. The receiver as recited in claim 8, wherein said first unit comprises a third unit configured to detect one of said inputs of said completion detector that has not changed state upon said completion detector generating said signal, wherein said one of said inputs that did not change state corresponds to a particular synchronization state / retiming state pair to be asserted.

10. The receiver as recited in claim 7, wherein each of said plurality of second units comprises circuitry for performing a NOR function on particular sampled phase values.

11. The receiver as recited in claim 8, wherein said completion detector comprises circuitry for performing a NOR function on said logical values of each particular synchronization state / retiming state pair outputted by said plurality of second units.

12. The receiver as recited in claim 1, wherein said oscillator operates at a frequency lower than a data rate of said serial data.

13. A system comprising:

a transmission medium;

a transmitter coupled to said transmission medium, wherein said transmitter is configured to transmit data in a serial form; and

a receiver coupled to said transmission medium, wherein said receiver is configured to receive said serial data, wherein said receiver comprises an oscillator configured to generate phases of a clock, wherein said receiver further comprises a retiming mechanism configured to receive said serial data and said phases of said clock, wherein said retiming mechanism includes circuitry for reducing timing uncertainties in said serial data by selecting a particular phase of said clock to be asserted to sample said serial data during a period of said serial data.

14. The system as recited in claim 12, wherein each particular phase of said clock to be asserted to sample said serial data during a particular period of said serial data corresponds to a particular retiming state.

15. The system as recited in claim 14, wherein each particular retiming state is paired with a particular synchronization state, wherein said particular synchronization state indicates which particular phase of said clock to assert at a given transition of said serial data signal.

16. The system as recited in claim 15, wherein said retiming mechanism comprises a first unit, wherein said first unit includes circuitry for generating logical values of each particular synchronization state / retiming state pair.

17. The system as recited in claim 16, wherein said first unit receives said phases of said clock and said serial data.

18. The system recited in claim 17, wherein said first unit comprises a sample clock mechanism configured to sample values of said phases of said clock.

19. The system as recited in claim 18, wherein said first unit comprises a plurality of second units, wherein said sampled phase values are inputted to said plurality of second units, wherein said plurality of second units includes circuitry for generating said logical values of each particular synchronization state / retiming state pair.

20. The system as recited in claim 19, wherein said plurality of second units output said logical values of each particular synchronization state / retiming state pair to a completion detector, wherein said completion detector includes circuitry for generating a signal indicating a time to sample inputs of said completion detector.

21. The system as recited in claim 20, wherein said first unit comprises a third unit configured to detect one of said inputs of said completion detector that has not changed state upon said completion detector generating said signal, wherein said one of said inputs that did not change state corresponds to a particular synchronization state / retiming state pair to be asserted.

22. The system as recited in claim 19, wherein each of said plurality of second units comprises circuitry for performing a NOR function on particular sampled phase values.

23. The system as recited in claim 20, wherein said completion detector comprises circuitry for performing a NOR function on said logical values of each particular synchronization state / retiming state pair outputted by said plurality of second units.

24. The system as recited in claim 13, wherein said oscillator operates at a frequency lower than a data rate of said serial data.